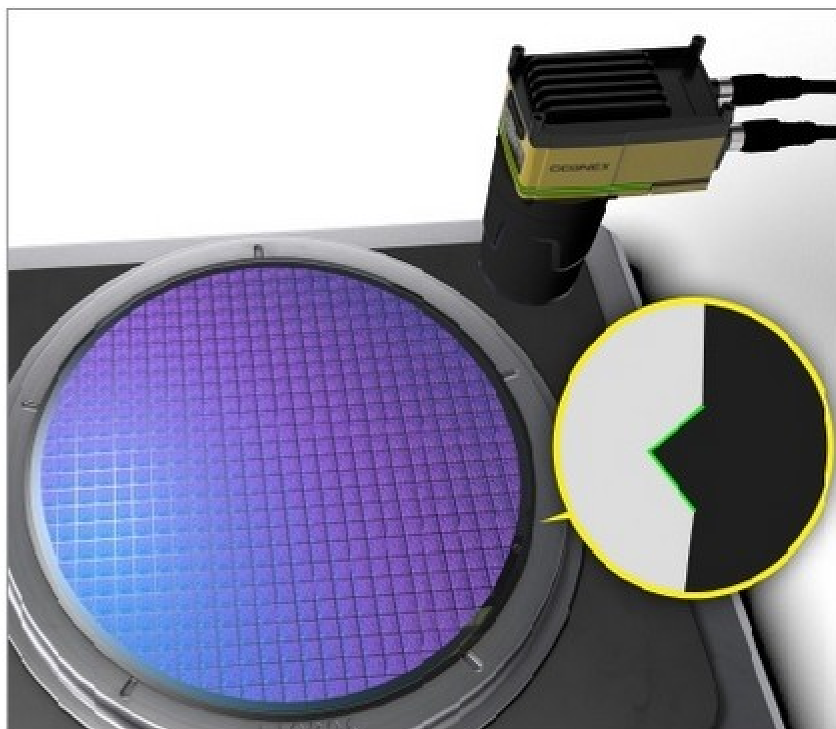
GAIN A COMPETITIVE EDGE IN SEMICONDUCTOR MANUFACTURING USING MACHINE VISION AND DEEP LEARNING

Rebounding demand for chips has severely strained manufacturing capacity worldwide. Anything that makes the process of chip manufacturing faster, more efficient, and cheaper delivers a competitive advantage.

Increasingly, sophisticated vision systems equipped with deep learning tools are showing the way to significant capacity improvements within short time horizons, improving alignment, traceability, and defect detection.

Alignment

Silicon wafers are manufactured in a series of steps, with each placing another layer of material over previous layers, and these layers must align precisely.



Wafer notch detection

Overall wafer alignment is often achieved by checking the orientation of a notch. Traditional methods are bulky, slow, and have trouble with increasingly common transparent wafers.

A Cognex In-Sight Vision system equipped with PatMax algorithms fits into tight spaces and reliably detects the notch in any orientation.

Wafer and die alignment

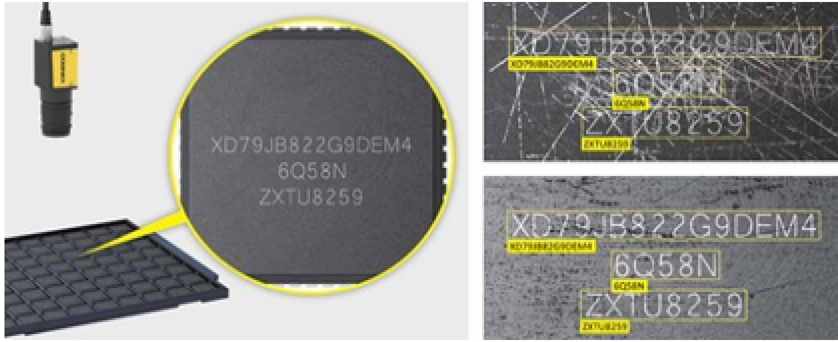
Poor wafer alignment causes problems during photolithography, probing and testing, and dicing, leading to defects and waste.

Cognex's PatMax's geometric pattern-finding algorithms locate and align variable wafer and die patterns with high accuracy and repeatability, improving quality and yield.

Identification/traceability

To ensure manufacturing efficiency, measure product quality, and combat counterfeiting, wafers, wafer carriers, lead frames, dies, integrated circuits (ICs), and printed circuit boards (PCBs) carry machine-readable identification codes and human-readable alphanumeric characters for tracking.

These codes can be hard to read or suffer wear during the manufacturing process, making optical character reading (OCR) and decoding difficult and error prone.



Wafer OCR

Laser-marked alphanumeric or Data Matrix IDs trace silicon wafers from creation to dicing. Wafer surfaces are reflective, and the code can be degraded during masking, etching, and photolithography.

Cognex wafer readers use wafer-specific detection algorithms for both OCR and 2D barcodes. Integrated adaptable lighting and image processing minimize no-reads.

Wafer carrier ring OCR

Since the laser-marked ID on the wafer itself becomes unusable after dicing, wafers are carried through dicing to wire bonding by an ID-marked carrier ring. Cleaning after dicing degrades the carrier ring codes, causing automation slowdowns when codes are misread.

Ambiguous alphanumeric characters and carrier ring surface variations make it difficult for traditional machine vision to recognize the codes. A smart camera with Cognex Deep Learning's OCR tool recognizes even severely damaged codes.

IC (Integrated Circuit) tracking

Chips in ICs are bonded to a metallic substrate, called a lead frame, for connectivity and support. Lead frames are laser scribed with 2D Data Matrix barcodes. Degradation during production and the low contrast and reflectivity of the lead frames themselves make these codes a challenge to read.

Cognex image-based barcode readers with flexible lighting and optics use industry-leading algorithms to decode even challenging 2D Data Matrix barcodes.

IC OCR

After package testing, each chip is stamped with an alphanumeric code for traceability and verification as chips are assembled on PCBs. These codes can be deformed by ambient lamination and highly textured surfaces, reducing readability.

Cognex Deep Learning's OCR tool is readily trained to read deformed, skewed, and low-contrast codes against reflective and textured backgrounds and can be quickly retrained on new surfaces.

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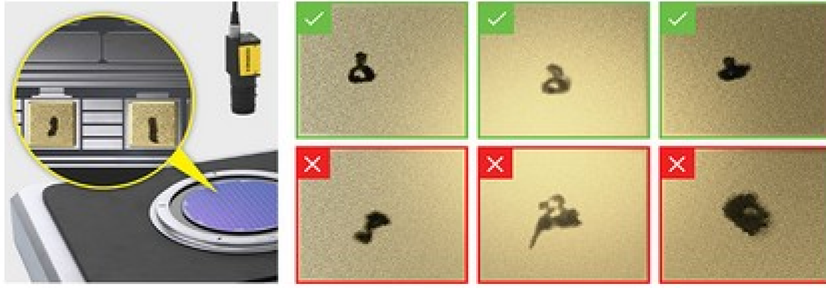
Defect inspection

Identifying defects early in the production process while passing purely cosmetic flaws increases yield rate per wafer by minimizing rework and manual inspection.



Wafer defect inspection

Each wafer layer must be inspected before the next is deposited. The range of defects is large and can appear anywhere against the background of previous layers.

Cognex Deep Learning's defect detection tool trains on an image set of defect-free layers and can then find and identify defects anywhere in the wafer layer and reject anomalies.

Probe marks

Probes used for wafer testing before die preparation leave marks whose shapes can reveal if the probe is exerting incorrect pressure on the wafers, an early sign of probe failure.

Cognex Deep Learning's classification tool can distinguish between the wide range of good and bad marks, allowing for early corrections to probes, increasing both probe life and wafer yields.

Die edge

Wafer dies may be chipped or have burrs along their kerfs. Such defects are variable and hard to consistently detect with traditional machine vision.

Cognex Deep Learning's classification tool distinguishes chipping and burr defects from the wide range of normal cut marks. It also detects gradual wear on the cutting blade, enabling replacement before error rates rise.

Die surface

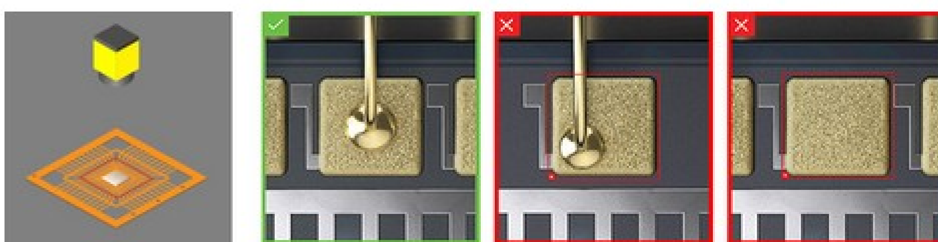
Each die, or chip, can have a wide range of significant surface defects, but also cosmetic flaws that do not affect function. It is difficult for both traditional machine vision and human inspectors to distinguish between them.

Cognex Deep Learning's defect detection tool detects and marks unacceptable anomalies while passing purely cosmetic defects.

Wire bonds

Wire bonding connects chips to lead frames, which then connect to other components. Defects can disrupt signal transmission. The range of defects is wide and can overlap with cosmetic defects that do not affect function.

A combination of Cognex Deep Learning's defect detection and classification tools can extract regions of anomalies and then distinguishes good from bad wire bonds.



WLCSP (Wafer Level Chip Scale Package) sidewall

Wafer Level Chip Scale Packages are a way of packaging an integrated circuit while it is still part of the wafer. Sidewall cracks can degrade performance, but layer boundaries and cracks can be hard to distinguish from each other.

Cognex Deep Learning's defect detection tool accurately distinguishes between sidewall cracks and layer boundaries.

IC (Integrated Circuit) molding

Integrated circuits are encapsulated in plastic to protect them. Various cracks, deformations, and voids can compromise protection, but the process can leave cosmetic defects that do not affect function.

Cognex Deep Learning's defect detection tool detects functional anomalies while passing purely cosmetic flaws. The classification tool can be used to identify specific defect types to address production issues.

IC (Integrated Circuit) leads

Missing or bent chip pins can render chips nonfunctional. The wide range of pin defects and locations challenge traditional machine vision.

Cognex Deep Learning's defect detection tool quickly detects anomalies and rejects chips with pin defects.

Improve semiconductor fabrication throughput with machine vision

Cognex machine vision systems, particularly when equipped with Cognex Deep Learning tools, improve silicon wafer alignment, enable accurate tracing of wafers and chips, and detect and classify a wide range of defects at every step from wafer to PCB (printed circuit boards). At minimal capital cost, improvements can be seen at every step of the semiconductor supply chain.

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